

**MANUFACTURE OF SEMICONDUCTOR DEVICE**

Patent Number: JP2238629  
Publication date: 1990-09-20  
Inventor(s): TSUKUDA KAZUAKI  
Applicant(s): FUJITSU LTD  
Requested Patent: ☐ JP2238629  
Application Number: JP19890059104 19890310  
Priority Number(s):  
IPC Classification: H01L21/3205  
EC Classification:  
Equivalents:

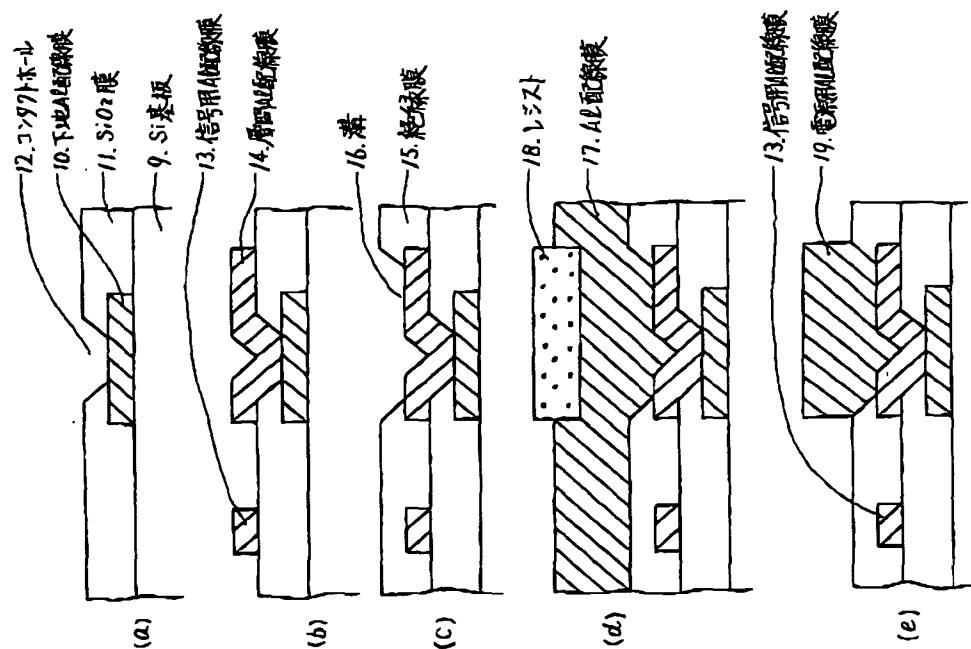
**Abstract**

**PURPOSE:**To reduce a difference in level of a multilayer wiring insulating layer, to increase an effect of a flattening operation and to enhance a coverage of a protective film by a method wherein a substratum wiring film for power- supply use and a wiring film for signal use are formed on an insulating film which has been applied to a substrate.

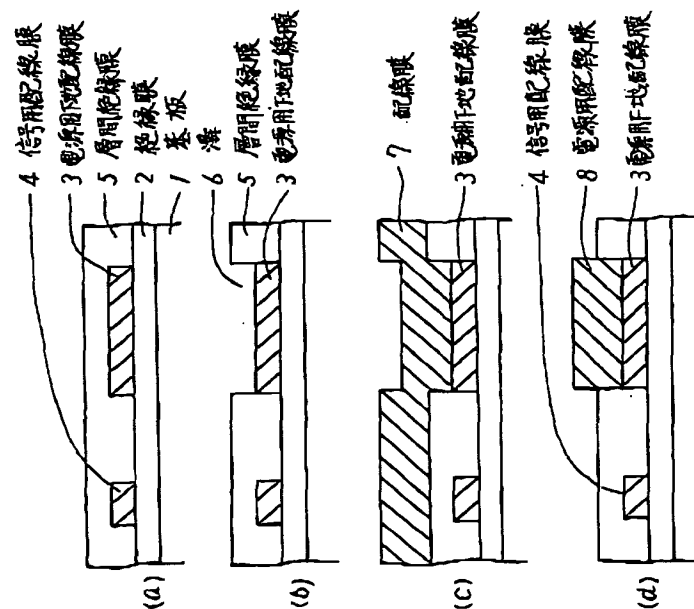
**CONSTITUTION:**A substratum wiring film 3 and a wiring film 4 for signal use are formed on a semiconductor-device substrate 1 where an element-wiring operation has been finished; after that, an interlayer insulating film 5 is coated on it. Then, only the interlayer insulating film 5 on the substratum wiring film 3 is removed; a groove 6 whose pattern is identical to a power-supply wiring pattern is formed in the interlayer insulating film 5 by using the substratum wiring film 3 as a stopper; a wiring film 7 is deposited. In addition, the wiring film 7 in a part other than the groove 6 is removed; a wiring film 8 for power- supply use is completed. Thereby, it is possible to reduce a depth portion of the groove at a difference in level by the thick power-supply wiring part. A coverage of a protective film is made good; reliability of a semiconductor device is enhanced.

Data supplied from the **asp@cenet** database - 12

特開平 2-238629(4)



本発明の一実施例の工程順模式断面図  
第2図



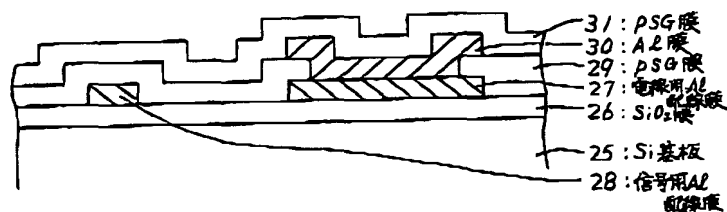
本発明の原理説明図  
第1図

特開平 2-238629(5)



一定施例中の絶縁膜平坦化の説明図

第3図



従来例の模式断面図

第4図